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(54) **DATA WRITE-IN DEVICEDATA WRITE-IN CONTROL METHODAND PROGRAM**

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a data write-in device and a data write-in control method for efficiently storing the same data in a plurality of storage devices including defective memory blocks.
SOLUTION: A NAND flash memory controller CN decides an address of a memory block having data to be written for each NAND flash memory based on a error flag stored in NAND flash memories N-1 to N-n (n: natural number). And decided each address is latched to a corresponding NAND flash memory to store the same part of data to be written in the NAND flash memories N-1 to N-nand the parts are supplied en bloc to the NAND flash memories N-1 to N-n. Addresses are latched dividing to a plurality of timesparts being common to a plurality of NAND flash memories are latched en bloc to the plurality of NAND flash memories out of a plurality of parts constituting each address.

CLAIMS

[Claim(s)]
[Claim 1]A data writing device characterized by comprising the following for storing the same data of each other in two or more memory storage which contains two or more memory block which was able to assign an addressrespectively.
A means to memorize the data concerned to memory block which was able to assign the address concerned when the target data written in after a store command and an address which direct an input of serial data are supplied is supplied to each memory storage and a write command which finally directs writing is supplied.
It is a thing provided with a means to supply error information which specifies poor memory blockAn address determination means to determine an address of memory block which memorizes the same data based on error information which acquired error information and was acquired from each memory storage for every memory storageAfter

supplying a store command to each memory storage and supplying each address determined as what shows each memory block which memorizes the same data according to memory storageA writing means which makes this each memory block memorize data by supplying the data concerned to each memory storage collectivelyand finally supplying a write command.

[Claim 2]Each memory storage divides supply of an address into pluralityreceives itand said writing meansThe data writing device according to claim 1 characterized by what a portion common to two or more memory storage is collectively supplied for to two or more memory storage concerned among two or more portions which constitute each address supplied according to memory storage.
[Claim 3]After each memory storage memorizes datathe data concerned is provided with a means to distinguish whether it is the no memorized normally and to notify a discriminated result to said writing meansand said writing meansWhen a discriminated result which shows that data is not memorized normally is notifiedThe data writing device according to claim 1 or 2 characterized by what memory block of an object which makes the data concerned newly memorize is determined from inside of memory block of memory storage which notified the discriminated result concernedand it has a means to make the memory block concerned memorize data which was not memorized normally for.
[Claim 4]When it distinguished whether said writing means would have the memory storage which runs short of memory block which should make data memorize and distinguishesThe data writing device according to claim 12or 3 characterized by what it has a means to stop making memory block of the memory storage concerned memorize data after the data concerned for.
[Claim 5]A data writing device given in any 1 paragraph of claims 1 thru/or 4 characterized by what said memory storage comprises NAND flash memory for.
[Claim 6]A data writing device given in any 1 paragraph of claims 1 thru/or 4 characterized by what said memory storage comprises an AND type flash memory for.
[Claim 7]A data write method characterized by comprising the following for storing the same data of each other in two or more memory storage which contains two or more memory block which was able to assign an addressrespectively.
A means to memorize the data concerned to memory block which was able to assign the address concerned when the target data written in after a store command and an address which direct an input of serial data are supplied is supplied to each memory storage and a write command which finally directs writing is supplied.
A means to supply error information which specifies poor memory block.

[Claim 8]When the target data written in after a store command and an address which direct an input of serial data for a computer are supplied is supplied and a write command which finally directs writing is suppliedA means to memorize the data concerned to memory block which was able to assign the address concernedError information is acquired from two or more memory storage respectively provided with a means to supply error information which specifies poor memory blockAn address determination means to determine an address of memory block which memorizes the same data for every memory storage based on acquired error informationAfter supplying a store command to

each memory storage and supplying each address determined as what shows each memory block which memorizes the same data according to memory storageA program for considering it as a writing means which makes data memorizeand making it function on this each memory block by supplying the data concerned to each memory storage collectivelyand finally supplying a write command.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention]This invention relates to the data writing device and the data write control method for writing the same data in two or more memory storage especially about a data writing device and the data write control method.
[0002]
[Description of the Prior Art]The flash memory is used as small memory storage. It divides roughly into a flash memory and there are a NOR typea NAND typeand an AND type in it. The random access in a 1-byte unit is possible for a NOR type flash memory. Howevercompared with a NAND type or an AND type flash memoryit is expensiveand a degree of location is low. On the other handsince a NAND type and an AND type flash memory are cheap compared with a NOR type flash memory and their degree of location is highit is used widely. As a NAND type flash memorythere is "TH58512FT" etc. by Toshiba Corp.for example.
[0003]
[Problem(s) to be Solved by the Invention]Howevera NAND type and an AND type flash memory are so large that they cannot disregard the rate of poor memory block (memory block which cannot memorize data normally) contained in the inside of memory block which constitutes a storage area. Thereforein order to write the same data in two or more NAND type (or AND type) flash memorieseven if it performs addressing in parallelwriting is not made normally in many cases.
[0004]For this reasonwhen the same data was written in two or more NAND type (or AND type) flash memoriescontrol signalssuch as a chip enable signalwere individually supplied to the flash memoryand data was written in each flash memory one by one.
[0005]Howeverwhen based on this techniquethe time taken to complete writing as the NAND type (or AND type) flash memory of the object which writes in data is extensive becomes very longand is inefficient-like. For this reasonit was very difficult conventionally to mass-produce the product containing the NAND type (or AND type) flash memory in which predetermined data was pre-installed.
[0006]This invention was made in view of the above-mentioned actual conditionand an object of an invention is to provide the data writing device and the data write control method for making the same data memorize efficiently to two or more memory storage which may contain poor memory block.
[0007]
[Means for Solving the Problem]In order to attain the above-mentioned purposea data writing device concerning the 1st viewpoint of this inventionTo two or more memory storage which contains two or more memory block which was able to assign an

addressrespectivelymutuallyare the same data a data writing device for making it memorizeand each memory storageWhen the target data written in after a store command and an address which direct an input of serial data are supplied is supplied and a write command which finally directs writing is suppliedA means to memorize the data concerned to memory block which was able to assign the address concernedIt is a thing provided with a means to supply error information which specifies poor memory blockAn address determination means to determine an address of memory block which memorizes the same data based on error information which acquired error information and was acquired from each memory storage for every memory storageAfter supplying a store command to each memory storage and supplying each address determined as what shows each memory block which memorizes the same data according to memory storageIt has a writing means which makes this each memory block memorize data by supplying the data concerned to each memory storage collectivelyand finally supplying a write command.

[0008]According to such a data writing devicememory block which makes data memorize was individually determined for every memory storageand also data which should be made to memorize is supplied collectively. Thereforeeven if such memory storage contains a defective blockit memorizes the same data efficiently. Serial data are not restricted to data transmitted one by one for every bitbut also contain in it data of the so-called data (data transmitted one by one for every byte) of byte serial compositionetc. transmitted one by one every two or more bits.

[0009]Each memory storage may divide supply of an address into pluralityand may receive it. In this casesaid writing means may supply a portion common to two or more memory storage to two or more memory storage concerned collectively among two or more portions which constitute each address supplied according to memory storage. Since the intersection also bundles up an address of memory block which makes data memorize by having such composition and it is supplied to two or more memory storagetime required in order to make data memorize is shortened further.

[0010]After each memory storage memorizes datait may be provided with a means by which the data concerned distinguishes whether it is the no memorized normallyand notifies a discriminated result to said writing means. In this casewhen a discriminated result which shows that data is not memorized normally is notified to said writing meansIf it shall have a means to make the memory block concerned memorize data which determined memory block of an object which makes the data concerned newly memorizeand was not normally memorized from inside of memory block of memory storage which notified the discriminated result concernedFor examplealso when memory block poor in late-coming arisesdata which failed in memory is certainly memorized by alternative memory block.

[0011]When it distinguished whether said writing means would have the memory storage which runs short of memory block which should make data memorize and distinguishesIf it shall have a means to stop making memory block of the memory storage concerned memorize data after the data concernedAlthough memory block which should make data memorize does not existit is avoided that useless processing which tries a data storage continuesand processing which makes data memorize becomes still more efficient.

[0012]Said memory storage may comprise NAND flash memoryfor exampleandspecificallymay comprise an AND type flash memory.

[0013]A data write control method concerning the 2nd viewpoint of this inventionTo two or more memory storage which contains two or more memory block which was able to assign an addressrespectivelymutuallyare the same data a data write method for making it memorizeand each memory storageWhen the target data written in after a store command and an address which direct an input of serial data are supplied is supplied and a write command which finally directs writing is suppliedA means to memorize the data concerned to memory block which was able to assign the address concernedIt is a thing provided with a means to supply error information which specifies poor memory blockAcquire error information from each memory storageand based on acquired error informationAn address of memory block which memorizes the same data is determined for every memory storageAfter supplying a store command to each memory storage and supplying each address determined as what shows each memory block which memorizes the same data according to memory storageThis each memory block is made to memorize data by supplying the data concerned to each memory storage collectivelyand finally supplying a write command.
[0014]According to such a data write control methodmemory block which makes data memorize was individually determined for every memory storageand also data which should be made to memorize is supplied collectively. Thereforeeven if such memory storage contains a defective blockit memorizes the same data efficiently.
[0015]A program concerning the 3rd viewpoint of this inventionWhen the target data written in after a store command and an address which direct an input of serial data for a computer are supplied is supplied and a write command which finally directs writing is suppliedA means to memorize the data concerned to memory block which was able to assign the address concernedError information is acquired from two or more memory storage respectively provided with a means to supply error information which specifies poor memory blockAn address determination means to determine an address of memory block which memorizes the same data for every memory storage based on acquired error informationAfter supplying a store command to each memory storage and supplying each address determined as what shows each memory block which memorizes the same data according to memory storageIt is characterized by being for considering it as a writing means which makes data memorizeand making it function on this each memory block by supplying the data concerned to each memory storage collectivelyand finally supplying a write command.
[0016]A computer which executes such a program determined individually memory block which makes data memorize for every memory storageand also it supplies collectively data which should be made to memorize. Thereforeeven if such memory storage contains a defective blockit memorizes the same data efficiently.
[0017]
[Embodiment of the Invention]Hereaftera flash memory write apparatus is explained for the data writing device and the data write control method concerning this embodiment of the invention as an example.
[0018](A 1st embodiment) Drawing 1 is a figure showing the composition of the flash memory write apparatus concerning a 1st embodiment of this invention. So that it may illustrate this flash memory write apparatusThe NAND flash memory controller CNthe bus B1and address latch enable signal line B-2-1 - B-2-n (total of the NAND flash memory which n mentions later)It comprises command latch enable signal line B3-1 -

B3-nlead enable signal line B4-1 - B4-nand lady signal wire B5-1 - B5-n. The bus B1 comprises the data / address busand the write enable signal wire which are connected common to n NAND flash memories N-1 which are the objects which write in data - N-n.
[0019]The NAND flash memory controller CN is connected to the data / address busand the write enable terminal which NAND flash memory N-1 - N-n mention later via the bus B1. The NAND flash memory controller CN is connected to the address latch enable terminal of NAND flash memory N-k via address latch enable signal line B-2-k (k is the arbitrary integers below or more 1n). The NAND flash memory controller CN is connected to the command latch enable terminal of NAND flash memory N-k via command latch enable signal line B3-k. The NAND flash memory controller CN is connected to the lead enable terminal of NAND flash memory N-k via lead enable signal line B4-k. The NAND flash memory controller CN is connected to the lady terminal of NAND flash memory N-k via lady signal wire B5-k.
[0020]The NAND flash memory controller CN comprises a control section and a storage parts store. The control section of the NAND flash memory controller CNIt comprises a CPU (Central Processing Unit) etc.and the program which controls the processing of data writing mentioned later is read and executed from the storage parts store of the NAND flash memory controller CN.
[0021]The storage parts store of the NAND flash memory controller CN comprises nonvolatile storagessuch as PROM (Programmable Read Only Memory)and volatile storagessuch as RAM (Random Access Memory). The nonvolatile storage with which the storage parts store of the NAND flash memory controller CN is providedThe above-mentioned program which controls processing of data writing is memorized beforehandand the volatile storage of the storage parts store of the NAND flash memory controller CN is used as a work area of the control section of the NAND flash memory controller CN.
[0022]NAND flash memory N-k (k is the arbitrary integers below or more 1n) comprises a NAND type EEPROM (Electrically Erasable/Programmable ROM).
[0023]Drawing 2 is a block diagram showing the composition of NAND flash memory N-k. So that it may illustrate NAND flash memory N-kData/address busan input-and-output control circuitand a command registerIt comprises a control circuita status registera logic control circuit of operationa memory cell arraya data registeran address registera row address buffera row address decodera column bufferand a column decoder.
[0024]It has connected with an external circuit and data/address bus has the bit width of two or more bits. An input-and-output control circuit receives a commanddataand an address from an external circuit via data/address busor sends them out to an external circuit. A command register keeps the command which the input-and-output control circuit received from the external circuit as a bit string. A control circuit controls operation inside NAND flash memory N-k as it is specified by the command kept by the command register. A status register notifies the result of the control which the control circuit performed to an external circuit. A logic control circuit of operation answers the signal supplied from an external circuitand controls operation of an input-and-output control circuit and a control circuit. The logic control circuit of operation is provided with a write enable terminalthe address latch enable terminalthe lead enable terminalthe command latch enable terminaland the lady terminal. A memory cell array comprises two or more memory cells mentioned later. A data register keeps the data of the object written

by reading and the memory cell. An address register memorizes the position (address) of the data of the object written by reading and the memory cell array. A row address buffera row address decodera column bufferand a column decoder change the two or more bits address which an address register memorizes into the line and sequence which specify a memory celland choose this memory cell.
[0025]Each memory cell of NAND flash memory N-k has a storage capacity of 1 byte. Logicallythese memory cells are arranged at the matrix form of the length of 131072 linesand 528 rows widefor exampleas shown in drawing 3. ThereforeNAND flash memory N-k has a storage capacity of about 69.2 megabytes as the whole.
[0026]Each line of the matrix of a memory cell constitutes the page which has a storage capacity of 528 bytes so that it may illustrate. The addresses from 1 to 528 are continuously given to the memory cell contained in each page. Each page constitutes one block from a head per 32 pages. Each block has a storage capacity of 16 K bytesand the whole storage area comprises 4096 blocks. The page addresses from 1 to 32 are continuously given to the page belonging to each block.
[0027]Each page comprises a data area which occupies 512 bytes of field from a headand a redundancy part which occupies 16 bytes of end so that it may illustrate. The address (physical address) of the data for reading and writing comprises a 26-bit bit stringfor example. 9 bits of low ranks of a physical address show the position (line number) of the line in which remaining top 17 bits have this memory cell in the position (aisle location) of a sequence with the memory cell by which this data is written. The ranges of an aisle location are 1-512and the ranges of a line number are 1-131072.
[0028]As for remaining top 12 bits5 bits of low ranks show the position (block position) of this block for the position (page position) which is a page to which this memory cell belongs within the block containing this memory cell among 17 bits which shows a line number. The ranges of a page position are 1-32and the ranges of a block position are 1-4096.
[0029]When writing dataflash memory N-k usually memorizes the address which shows the aisle location "0"and write data from the head of a page. [reading and] As a result of carrying out like thisreading and flash memory N-k write data from the head of a data area. The arbitrary data of the user datum which a user usesthe device driver which the device of the exterior which accesses NAND flash memory N-k performsetc. is stored in a data area.
[0030]On the other handthe error check code for checking that the contents of the data (an user datuma device driveretc.) stored in the data area of the page concerned are not destroyed according to the processing mentioned later is stored in the redundancy part of each pageand an error flag is further stored in it. An error flag needs to be stored in no pages of each blockfor examplemay be stored only in the redundancy part of the page (getting it blocked the 1st page) of the head of each block.
[0031]The block of an error flag with which this error flag is stored data. [whether it is a storable block (excellent article block) normally and] . [whether it isthe blocki.e.the defective blockwhich are not excellent article blocksand is the block (initial failure block) judged to be poor by the manufacturer of NAND flash memory N-ketc. before shipmentand] It is data in which it is shown whether it is a defective block and is the block (late-coming defective block) judged that it cannot perform normal storing of data while using NAND flash memory N-k.

[0032]Howeveran error flag may be used in order to show the attribute of the data in a data area combining other flags stored in the redundancy part as indicatedfor example by the application for patent 2001-076945.
[0033]By not eliminating data but only overwritingthe value of the error flag which shows an excellent article block is chosen so that updating to the value showing a late-coming defective block may be attained. An error flag shall specifically comprise 1 byte (8 bits) of a bit stringfor example. When there are 7 bits or more of bits which show the value "1" among this bit stringan error flag shall show an excellent article blockand at the time of 2 bits or more of 6 bits or lesswhen the bit which shall show a late-coming defective block and shows the value "0" is 7 bits or morean initial failure block shall just be shown. If set in this waythe error flag which shows an excellent article block can be updated by not eliminating the memory value of the memory cell of a redundancy partbut overwriting from "1" to "0" so that a late-coming defective block may be expressed.
[0034]when read-out of data was directedread-out was directed to NAND flash memory N-k -- the data of a line -- one memory cell (namely1 byte) from a head -- every -- it reads in 528 steps and has a function supplied one by one from data/address bus. Directions of read-out of data supply a read command to data/address busfor examplenextthe address bit string (a block address.) used as the physical address which reads to data/address bus and specifies the memory cell of the target head 1 page (.) which supplied what combined the page address and the column address and as which NAND flash memory N-k was specified Or it carries out by supplying a lead enable signal to a lead enable terminal after checking having kept the data after the column address specified among the specified pages to the data registerand having made the lady signal into an active level.
[0035]NAND flash memory N-k eliminates a memory content by a block unit. If the address of a block of the object which eliminates a memory content is supplied to NAND flash memory N-k following the deletion command it is directed that eliminates the memory content of a block and an elimination execute command is supplied furtherThe memory content of all the memory cells contained in the block concerned is reset (specificallythe memory value of each memory cell is set to "1").
[0036]On the other handif a predetermined store command is supplied to data/address busNAND flash memory N-kThe time of each both sides of the below-mentioned WE (WriteEnable) signal supplied to a write enable terminal and the below-mentioned ALE (Address Latch Enable) signal supplied to an address latch enable terminal reaching an active level is detected. And it is a physical address for data writing (in detail) about the address information currently supplied to data/address bus when it detects. It latches as a bit string showing a part of address bit string which combined the block addressthe page addressand the column address showing the head byte in a page. And after thatif a bit string is latched 4 timeswhenever WE signal reaches an active level in the state of a non-active levelan ALE signalEvery 1 byte of data for [which was supplied to data/address bus] writing is memorized to the data register of NAND flash memory N-k.
[0037]If a predetermined write command (or program commands) is supplied to data/address bus after the data for [for 1 page] writing is memorized by the data registerNAND flash memory N-k is memorized to the memory cell after the memory cell the physical address of the data writing management expressed by four latched bit strings indicates the data for writing currently kept by the data register to be.

[0038](Operation of a 1st embodiment)next processing of this flash memory write apparatus are explained with reference to drawing 4. Drawing 4 is a flow chart which shows processing of data writing.
[0039]When this flash memory write apparatus starts processing of data writingfirst the NAND flash memory controller CNIt points to data read to NAND flash memory N-1 - N-nand the error flag stored in the redundancy part of NAND flash memory N-1 - the storage area of N-n is read. And based on the value which the error flag which the NAND flash memory controller CN read showsthe data (table) showing the block address of all the excellent article blocks in NAND flash memory N-1 - the storage area of N-n is created and memorized (drawing 4Step S1).
[0040]Nextthe NAND flash memory controller CN declares use of variable DATA# (it is got blocked and the storage area for storing the value of variable DATA# is secured in the storage area of the volatile storage with which a self storage parts store is provided). And the value "0" is stored in variable DATA# (Step S2).
[0041]Furthermorethe NAND flash memory controller CNBy securing the storage area for storing the data for 1 block written in NAND flash memory N-1 - N-n in the storage area of the volatile storage with which a self storage parts store is providedand controlling the circuit for storage controls which is not illustratedThe write data for 1 block is stored to the secured storage area (data storage field) (Step S3).
[0042]Nextthe NAND flash memory controller CN **********s the value of variable DATA# only 1 (step S4). Subsequentlyit is determined in which block of NAND flash memory N-1 - N-n the NAND flash memory controller CN writes data with reference to a table based on current value d of variable DATA# (Step S5).
[0043]When processing of Step S5 is explained still more concretelythe NAND flash memory controller CN firstWith reference to a tablea block address specifies the block address of a small excellent article block as the d-th about NAND flash memory N-k (k is the arbitrary integers below or more 1n).
[0044]Nextthe NAND flash memory controller CN declares use of variable PAGE# (it is got blocked and the storage area for storing the value of variable PAGE# is secured in the storage area of the volatile storage with which a self storage parts store is provided). And the value "0" is stored in variable PAGE# (Step S6).
[0045]Furthermorethe NAND flash memory controller CN specifies the address with which the head of the portion which should be stored in the page which variable PAGE# shows among the data for 1 block stored by the data storage field is stored (Step S7).
[0046]Nextthe NAND flash memory controller CNBy sending out a store command (Coms) to NAND flash memory N-1 - the data/address bus of N-n via the bus B1The preparations which write in NAND flash memory N-1 - the data register of N-nand store 1 page of the target data in NAND flash memory N-1 - N-n are made.
[0047]Thenthe NAND flash memory controller CNThe address bit string (physical address) which combined the block address specified by variable DATA#the page address specified by variable PAGE#and the column address showing the head in a page is made to latch to NAND flash memory N-k in 4 steps. Specifically the NAND flash memory controller CNIn order to make an address latch to NAND flash memory N-kthe bit string which constitutes a part of physical address is sent out to data/address busIn this statefurtherthe ALE signal of an active level is supplied to NAND flash memory N-k via address latch enable signal line B-2-kand WE signal of an active level is supplied to

NAND flash memory N-1 - N-n via the bus B1.
[0048]As for NAND flash memory N-kthe data sent out to data/address bus when both the ALE signal supplied to self and WE signal serve as an active level is latched as a bit string showing a part of physical address.
[0049]Namelyas shownfor example in drawing 5after the store command (data shown as "Coms" by drawing 5) was sent outWhen making one of the bit strings which should be made to latch to NAND flash memory N-1 (data shown as "add (1)" by drawing 5) latch[when both of ALE signals (signal shown as "an ALE signal (B-2-1)" by drawing 5) supplied to WE signal and address latch enable signal line B-2-1 reach an active level (signal level shown with a dashed line by drawing 5)]This bit string ("add (1)") is sent out to Buss B1.
[0050]When making one of the bit strings which should be made to latch to NAND flash memory N-k (data shown as "add (k)" by drawing 5) similarly latchWhen both of ALE signals (signal shown as "an ALE signal (B-2-k)" by drawing 5) supplied to WE signal and address latch enable signal line B-2-k reach an active levelthe bit string "add (k)" is sent out to the bus B1.
[0051]The NAND flash memory controller CNWhen the bit string made to latch to two or more NAND flash memories is commonthe timing of sending out of each bit string shall be adjusted so that it may be latched to these NAND flash memories to the timing that if possible this common bit string is the same.
[0052]When making the bit string (data shown as "add (n)" by drawing 5) which should be made to latch common to NAND flash memory N-1 and N-n specifically latch as shownfor example in drawing 5WE signalWhen each of ALE signals (B-2-1) and ALE signals (signal shown as "an ALE signal (B-2-n)" by drawing 5) supplied to address latch enable signal line B-2-n reaches an active levelthe bit string "add (n)" is sent out to the bus B1.
[0053]The physical address of the data for writing consists of a bit string which is 26 bits more concretelyfor exampleThe aisle location (1-512) of the memory cell of the target head where 9 bits of low ranks of this bit string write in data is shownand top 17 bits presupposes that the line number (1-131072) of this memory cell is shown. 5 bits of low ranks of the 17-bit bit string which shows a line number presuppose that the page position (1-32) of this memory cell is shownand top 12 bits shows a block position (1-4096). And it is assumed that 8 bits of low ranks of the aisle location of the memory cell of the object which writes in data are common in all n NAND flash memoriesand no less than top 10 bits of a block position are common in all NAND flash memories. About 2 bits of low ranks of top 1 bit of the aisle location of a memory cell5 bits which shows a page positionand a block positiona value presupposes that there are 3 sets of groups of a common NAND flash memory. In this casethe NAND flash memory controller CNFor example(1) 8 bits of 1st low rank of the aisle location of the memory cell of the object which writes in data is sent out in common with all n NAND flash memoriesIn the 2nd time - the 4th time(2) Top 1 bit of the aisle location of this memory cell2 bits of low ranks of the page position of 5 bitsand a block position Every 1 time per group of a NAND flash memory with these common valuesIt sends out a total of 3 timesand is (3). The 5th timeEight of top 10 bits of a block position is sent out in common with all the NAND flash memoriesand it is (4). The 6th timeThe timing of sending out of each bit string is adjusted with the technique of sending out remaining 2 bits of the bit string

which shows a block position in common with all the NAND flash memories.
[0054]By adjusting such timingthe NAND flash memory controller CN shortens time to spend in order to make a physical address latch to NAND flash memory N-1 - N-n.
[0055]The concrete numerical value mentioned above in order to explain the transmission timing of a bit string is illustrated in order to make an understanding of this embodiment easyand a numerical combination is not limited to what was mentioned above.
[0056]Thenthe NAND flash memory controller CNIn order to write data in NAND flash memory N-1 - N-nEvery 1 byte of data for 1 page after the head position as which the address was specified among the data for 1 block stored by the data storage field is sent out to subsequent data/address bus from a headWhenever it sends out 1 byteWE signal of an active level is supplied to NAND flash memory N-1 - N-n. As a resultNAND flash memory N-1 - N-n keep the data for 1 page to each one of data registers.
[0057]Nextthe NAND flash memory controller CN sends out a write command (data shown as "Comw" by drawing 5) via the bus B1 to NAND flash memory N-1 - the data/address bus of N-n. If a write command is receivedNAND flash memory N-1 - the control circuit of N-n will start writing operationand will change a lady signal into an inactive state. As a resultNAND flash memory N-1 - N-n memorize a part for the one-page data for [which is kept to the data register at the memory cell which is a page which the physical address which each one latched most newly shows] writing (Step S8).
[0058]Each control circuit of NAND flash memory N-1 - N-n writes in inspecting the success or failure of the writing of datawhen writing the data for 1 page in a memory cell from a data register. It is inspected whether the memory content of the memory cell was compared with the memory content of the data registerand data was specifically correctly memorized by the memory cell by the writing operation within time predetermined in dataand within prescribed frequencyfor example. When it does not memorize correctlydata writing failure (Fail) is shownand when it memorizes correctlythe status bit which shows a data writing success (Pass) is stored in a status register. And an end of the writing of the data for 1 page will make a lady signal an active state.
[0059]The NAND flash memory controller CNIt checks that NAND flash memory N-1 - the lady signal of all N-n have been in the active stateand a status read command is sent out to NAND flash memory N-1 - the data/address bus of N-n via the bus B1.
[0060]Nextthe NAND flash memory controller CN makes an active state the lead enable signal of NAND flash memory N-kand reads a memory content for the status register of NAND flash memory N-k.
[0061]The NAND flash memory controller CN reads the memory content of a status register by above-mentioned operation about all NAND flash memories N-1 - N-nand moves processing to Step S10 (step S9).
[0062]The NAND flash memory controller CNby being alikeif the memory content of NAND flash memory N-1 - all the status registers of N-n is a write-in success (when the specific bit showing "Pass" in a status register is specifically a predetermined active statefor example)it will move processing to Step S11.
[0063]on the other handthe memory content of the status register of either NAND flash memory N-1 - N-n is alikeand a write-in failure. If it is (a case where the bit showing "Pass" in a status register is specifically in the inactive statefor example)processing will be moved to Step S13 noting that late-coming is poor as for the block of an applicable

NAND flash memory (Step S10).
[0064]At Step S11the NAND flash memory controller CN distinguishes whether the page which finally wrote data in NAND flash memory N-1 - N-n is a page of the end of a block based on the value of variable PAGE#.
[0065]If the value of variable PAGE# is less than "31" when the blocks of NAND flash memory N-1 - N-n consist of 32 pagesfor examplespecificallyIt judges that there is a page by which data has not been written yet in the block which is a present write-in objectand processing is moved to Step S16. On the other handif the value of variable PAGE# is "31"it will judge that the page which finally wrote in data is a page of the end of the block which is a present write-in objectand processing will be moved to Step S12.
[0066]At Step S16when only 1 **********s the value of variable PAGE#the NAND flash memory controller CN makes the preparations which write data in the next pageand moves processing to Step S7.
[0067]At Step S12the NAND flash memory controller CNIf it distinguishes having returned processing to Step S3 and having been written inwhen it did not distinguish and write in whether all the data that should be written in NAND flash memory N-1 - N-n was written in and having been distinguishedprocessing of data writing will be ended.
[0068]At Step S13the NAND flash memory controller CN specifies the block of the NAND flash memory (belowthis NAND flash memory is explained as what is NAND flash memory N-k) used as a write-in failure with a late-coming defective block. The value of variable PAGE# which expresses with Step S8 the page which wrote in most newly is specified.
[0069]Nextthe NAND flash memory controller CN writes the error flag which shows that this block is a late-coming defective block in the redundancy part of each page within the block with which data contains the page of NAND flash memory N-k which was not written in normally. Howeverit may be made to write an error flag only in the redundancy part of the page of the head of this block instead of writing an error flag in all the pages of this block. By carrying out like thisthe time of the writing which shows that this block is a late-coming defective block can be shortened.
[0070]Thendata is a form where the data showing the block of NAND flash memory N-k which was not written in normally is exceptedand the NAND flash memory controller CN updates a table (Step S14). (or again creation)
[0071]Thenthe NAND flash memory controller CNBased on the table updated (or again creation)the d-th excellent article block of NAND flash memory N-k and the block which became are specifiedThe data written in by the page which variable PAGE# specifies as the specified block from the page of the head of the block which variable DATA# shows is written in one by one by performing the same processing as Step S8. And in order to perform the writing to NAND flash memory N-1 - the remaining pages of N-nprocessing is moved to Step S11 (Step S15).
[0072]As a result of performing processing of Steps S1-S16 explained abovethe same data of each other is written in NAND flash memory N-1 - N-n. At the time of the writing processing to the excellent article block newly selected at Step S15after writing in to a pagethe success or failure of writing are inspected like step S9and when it is judged as a write-in failureit may be made to perform processing after Step S13 again. If it carries out like thisalso when a late-coming defective block occurs continuouslyan alternative block can be specifiedand more efficient writing can be performed.

[0073]The composition of this flash memory write apparatus is not restricted to an above-mentioned thing. For examplethe size of each block of NAND flash memory N-k is not restricted to an above-mentioned size. For exampleeach block does not need to comprise 32 pagesfor exampleshould just be an integral multiple of the size of each page. The number of times which latches the bit string which constitutes one physical address is not restricted to the above-mentioned number of timeseither. The number of the number of blocks and the memory cells per page and the number of redundancy parts with which NAND flash memory N-k is provided are also arbitrary.
[0074]Each block of flash memory N-k is classified further in further two or more zonesa potato is good and the zone address may be given to each zone. In this casethe table which the NAND flash memory controller CN creates in processing of data writing (updatingre-creation)What is necessary is just to make it comprise data showing the block address and zone address of the excellent article block in NAND flash memory N-1 - the storage area of N-n.
[0075]The NAND flash memory controller CN acquires the data written in NAND flash memory N-1 - N-n according to an operator's operationor itOr acquire by reading in the recording medium with which self was equippedor. Or in this case that it may be made to acquire by receiving from an external system via a communication line the NAND flash memory controller CNFor examplethe recording medium driver which reads a keyboard and the data from a recording medium. (For examplea flexible disk drive unit and MO (Magneto Optical disk) drive device) What is necessary is just to have the input part which consists of a serial port for performing communication with the exterioretc.
[0076]The initial value substituted for the above-mentioned step S2 at variable DATA#It is not necessary to be necessarily "0" for exampleand it is good also as an initial value of variable DATA#and a number only with larger 1 than the block address of a block of the end of NAND flash memory N-kOr it is good also considering the arbitrary offset values below the block address of a block of the end of NAND flash memory N-k as an initial value of variable DATA#.
[0077]What is also done for a decrement (only 1 specifically decreases the value of variable DATA#) does not interfere instead of **********ing variable DATA#.
[0078]The NAND flash memory controller CNFor examplea table is referred to in the above-mentioned step S12When it distinguished whether some in which memory block with possible making data memorize does not remain would be in the inside of NAND flash memory N-1 - N-n and distinguishesit may be made to interrupt processing of data writing. It is avoided by carrying out like this that useless processing follows. what was carried out as for the proposal exception when memory block with possible the NAND flash memory of the object which interrupts processing of data writing making data memorize did not remain -- good -- it may carry out and they may be all n NAND flash memories N-1 - N-n.
[0079]When writing in the data for 1 pagein the operation mentioned aboveit is writing data each in the data area and redundancy part of the same page by one processing of Steps S8 and S15. Howeverit may be made to write in data by performing Steps S8-S10 and processing of S13-S15 separately about each of a data area and a redundancy part. After inspecting the success or failure of the writing of a data area by carrying out like thisregardless of an inspection result (is it a late-coming defective block or not?)the writing of data is made to a redundancy part. According to this techniqueit becomes easy

to write in the redundancy part of a NAND flash memory and use a special flag etc.
[0080]The 2nd embodiment flash memory write apparatus of this invention that writes in (a 2nd embodiment)next the data to a NAND flash memory is explained. Drawing 6 is a figure showing the composition of this flash memory write apparatus.
[0081]As shown in drawing 6this flash memory write apparatusThe point which replaces with the NAND flash memory controller CNand is provided with NAND flash memory controller CAThe point which replaces with the bus B1 and is provided with bus B6and the point which replaces with address latch enable signal line B-2-1 - B-2-nand is provided with write enable signal wire B7-1 - B7-nInstead of not having command latch enable signal line B3-1 - B3-nAn address latch enable signal and a command latch enable signal are substantially [as the composition shown in drawing 1 except for the point transmitted by bus B6 as NAND flash memory N-1 - a bus signal common to N-n] the same. The composition of NAND flash memory A-k is substantially [as NAND flash memory N-k] the same.
[0082]NAND flash memory controller CA shall be connected to the data/address busaddress latch enable terminaland command latch enable terminal of n NAND flash memories A-1 which are the objects which write in data - A-n via bus B6. NAND flash memory controller CAIt is connected to the lead enable terminal of NAND flash memory A-k via lead enable signal line B4-kand via lady signal wire B5-kIt shall be connected to the lady terminal of NAND flash memory A-kand shall be connected to the write enable terminal of NAND flash memory A-k via write enable signal wire B7-k.
[0083]If a store command (Coms) is supplied to data/address busNAND flash memory A-kIt latches as a bit string showing a part of block address of the block of the data currently supplied to data/address bus when the time of WE signal supplied to a write enable terminal reaching an active level is detected and detected for data writing. And if a bit string is latched 4 timeswhenever WE signal will reach an active level after thatevery 1 byte of data for [which was supplied to data/address bus] writing is memorized to the block which the block address expressed by four latched bit strings shows.
[0084]Except for the point which is as the data writing processing which NAND flash memory controller CA is physicaland performs functional composition being the after-mentionedit is substantially [as the composition of the NAND flash memory controller CN] the same.
[0085](Operation of a 2nd embodiment) The processing of data writing which NAND flash memory controller CA and NAND flash memory A-1 - A-n of a flash memory write apparatus of drawing 5 performIt is substantially [as the processing which the NAND flash memory controller CN and NAND flash memory N-1 - N-n of the processing shown in drawing 3i.e.the composition of drawing 1perform] the same.
[0086]Howeverat Steps S8 and S15 NAND flash memory controller CAIn order to make the physical address specified as a physical address of the page which writes in data latchSend out the bit string which makes a part of this physical address to data/address busand send out an address latch enabling (ALE) signal to bus B6 further in this stateand. WE signal of an active level shall be supplied to NAND flash memory A-k via write enable signal wire B7-k. And as for NAND flash memory A-kthe data sent out to data/address bus when each of ALE signals supplied to self and WE signals serves as an active level shall be latched as a bit string showing a part of physical address.
[0087]Namelyas shownfor example in drawing 7after the store command "Coms" was

sent outWhen making one of the bit strings which should be made to latch to NAND flash memory A-1 (data shown as "add (1)" by drawing 7) latchWhere the address latch enabling (ALE) signal of bus B6 is held at an active level (signal level shown with a dashed line by drawing 7)When WE signal (signal shown as "a WE signal (B7-1)" by drawing 7) supplied to write enable signal wire B7-1 reaches an active levelthis bit string "add (1)" is sent out to bus B6 as data/an address signal.
[0088]When making one of the bit strings which should be made to latch to NAND flash memory A-k (data shown as "add (k)" by drawing 7) latch[where the ALE signal of bus B6 is held at an active levelwhen WE signal (signal shown as "a WE signal (B7-k)" by drawing 7) supplied to write enable signal wire B7-k reaches an active level]The bit string "add (k)" is sent out to bus B6 as data/an address signal.
[0089]When the bit string made to latch to two or more NAND flash memories is common like [NAND flash memory controller CA] a 1st embodimentThe timing of sending out of each bit string shall be adjusted so that it may be latched to these NAND flash memories to the timing that if possible this common bit string is the same. By carrying out like thisNAND flash memory controller CA shortens time to spend in order to make a block address latch to NAND flash memory A-1 - A-n.
[0090]Namelywhen making the bit string (data shown as "add (n)" by drawing 7) which should be made to latch common to NAND flash memory A-1 and A-n latch as shownfor example in drawing 7The ALE signal of bus B6 is in the state held at the active levelandmoreoverWE signal (B7-1)When each WE signal (signal shown as "a WE signal (B7-n)" by drawing 7) supplied to write enable signal wire B7-n reaches an active levelthe bit string "add (n)" is sent out to bus B6 as data/an address signal.
[0091]The composition of this flash memory write apparatus is not restricted to an above-mentioned thing. For exampleNAND flash memory A-1 - A-n may comprise AND flash memories (for exampleHitachi12811 [HN29W] etc.).
[0092]There is a flash memory with the composition which controls enabling/disable of input and output of a flash memory by a chip enable (CE) signal. In order to write data in such a flash memoryit may have the composition to which CE signal is used for instead of an ALE signaland a physical address is made to latch.
[0093]There is a flash memory with the composition which does not receive supply of an ALE signal but controls the latch of a physical address only by WE signal. In order to write data in such a flash memorya physical address may be made to latch using WE signal not using an ALE signaland it may have the composition which controls reading and writing of data using a serial clock signal.
[0094]In additionthe composition of the flash memory write apparatus concerning an embodiment of the invention is variously applicable within the limits of the main point of this invention.
[0095]As mentioned abovealthough this embodiment of the invention was describedthe data writing device of this invention cannot be based on a system for exclusive usebut can be realized using the usual computer system. the medium (a flexible disk.) which specifically stored the program for performing operation of the above-mentioned NAND flash memory controller CN in the computer to which the NAND flash memory was connectedfor example Install the program concerned from CD-ROM etc.orBy installing the program concerned from the medium which stored the program for performing operation of above-mentioned AND flash memory controller CA in the computer to

which the AND flash memory was connectedThe flash memory write apparatus which performs above-mentioned processing can be constituted.
[0096]For examplethe program concerned is put up for the bulletin board (BBS) of a communication networkThe modulated wave obtained by modulating a subcarrier with the signal which may distribute this via a communication line andwith which the program concerned is expressed is transmittedand the device which received this modulated wave restores to a modulated waveand it may be made to restore the program concerned. And above-mentioned processing can be performed by starting the program concerned and performing like other application programs under control of OS.
[0097]When OS shares a part of processingor when OS constitutes a part of one component of the invention in this applicationthe program except the portion may be stored in a recording medium. Also in this casethe program for performing each function or step which a computer performs shall be stored in that recording medium by this invention.
[0098]
[Effect of the Invention]As explained aboveaccording to this inventionthe data writing device and the data write control method for storing the same data in two or more memory storage which may contain poor memory block efficiently are realized.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1]It is a figure showing the basic constitution of the flash memory write apparatus concerning a 1st embodiment of this invention.
[Drawing 2]It is a block diagram showing the physical configuration of a flash memory.
[Drawing 3]It is a figure showing the logical configuration of the storage area of a flash memory.
[Drawing 4]It is a flow chart which shows processing of data writing.
[Drawing 5]A NAND flash memory controller is a timing **** figure which supplies a block address and data.
[Drawing 6]It is a figure showing the basic constitution of the flash memory write apparatus concerning a 2nd embodiment of this invention.
[Drawing 7]An AND flash memory controller is a timing **** figure which supplies a block address and data.
[Description of Notations]
CNa CA NAND flash memory controller
N-1 - N-n and A-1 - an A-n AND flash memory
B1 and B6 Bus
B-2-1-B-2-n Address latch enable signal line
B3-1-B3-n Command latch enable signal line
B4-1 - a B4-n lead enable signal line
B5-1-B5-n Lady signal wire
B7-1-B7-n Write enable signal wire